IDEC Chip Design Contest

An Electrical Stimulation IC with Chopped Pulse based Active Charge Balancing

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▪ MOTIVATION

- Neural stimulators can be used for the treatment of neurological disorders such as epilepsy, Parkinson's disease, and Alzheimer's, as well as to help restore body impairments such as in retinal and cochlear implants [1, 2]. In this work, an implantable HV compliance current mode neural stimulator integrated circuit (IC) using novel active charge balancing technique is proposed. The proposed charge balancing technique using chopped pulse waveform can minimize the amount of residual potential at the electrode. The stimulator IC designed using 0.18-µm standard CMOS process achieves 12.3 V of voltage compliance without reliability issue and can limit the electrode residual potential to a negligible level. All circuit functions are integrated on-chip without external components, and the fabricated chip consumes only 0.095 mm^2 of active area.

▪ CIRCUIT DESIGN

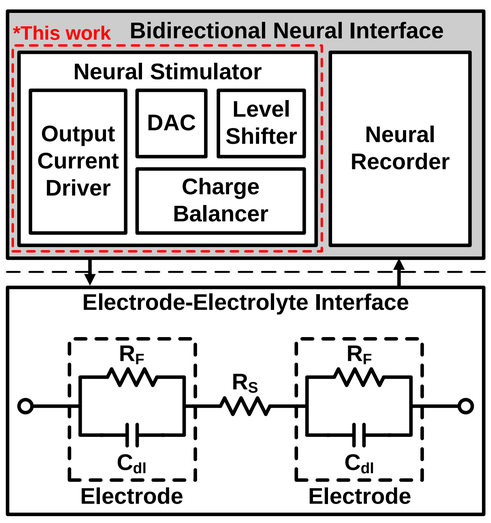

Fig 1. Block Diagram of stimulator IC

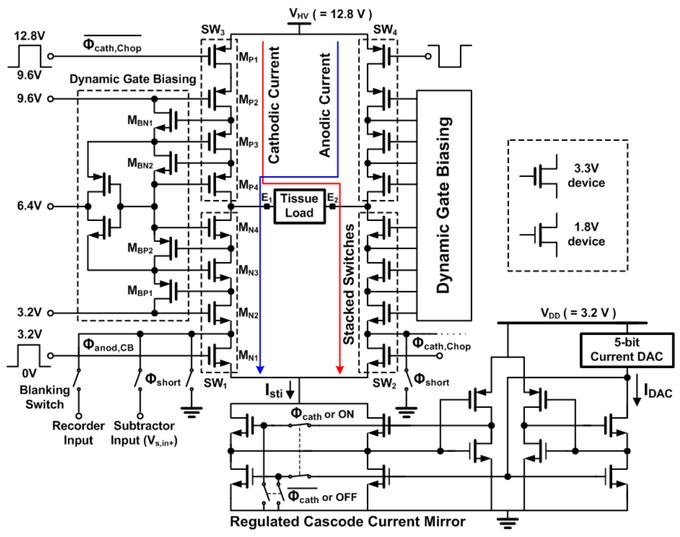

Fig 2. Proposed output driver

- Figure 1 shows the block diagram of the proposed stimulator system architecture and the equivalent electrode model used in the design. The stimulator system is comprised of a current-steering digital-to-analog converter (DAC), level-shifter, output current driver, and charge balancer circuits.
- Figure 2 shows the schematic of the regulated cascode current mirror and the output current driver used in the proposed stimulator IC. In the regulated cascode current mirror circuit, 1.8-V devices and 3.3-V devices are appropriately used for high output resistance and low voltage headroom. High supply voltage greater than 10 V is required to deliver up to 1 mA of current to 10 kΩ of tissue load. Each switch is implemented by four stacked 3.3-V transistor devices. The stacked devices are biased through the dynamic gate biasing circuit to keep the voltage across each terminal within 3.2 V to prevent breakdown due to the high supply voltage

▪ SIMULATION/EXPERIMENTAL RESULTS

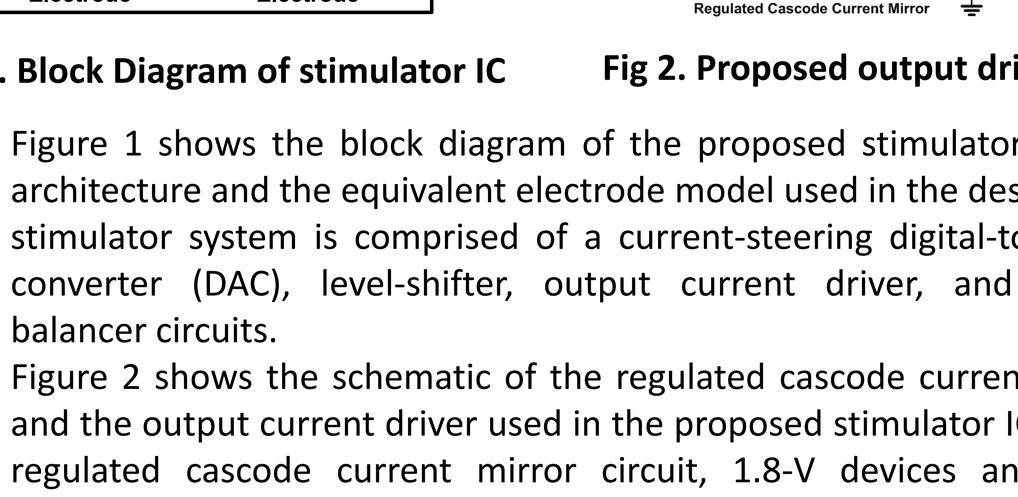

Fig 3. Measured stimulation voltage across electrode equivalent model load

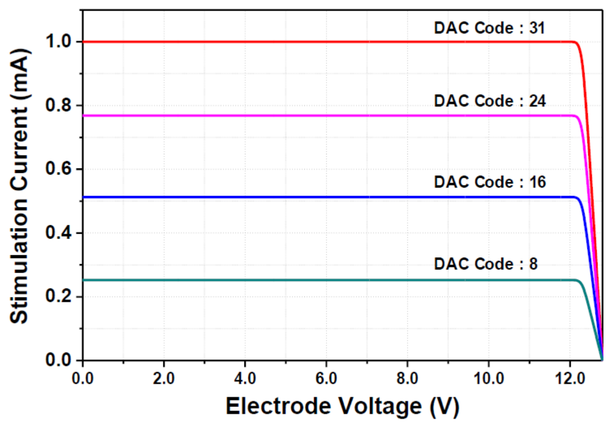

Fig 4. Measured voltage compliance

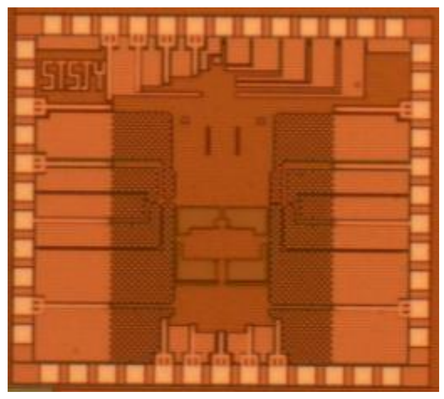

Fig 5. Chip Micrograph

- Figure 3 shows the measured stimulation voltage across electrode equivalent model with enabled active charge balancing and electrode shorting. Figure 4 shows measured voltage compliance for different DAC codes. Figure 5 shows the chip micrograph.

▪ PERFORMANCE SUMMARY

Parameter	This work	[2]	[3]	[4]
Voltage Compliance	12.3 V	12.3 V	< 20 V	< 20 V
Maximum Stimulation Current	1 mA	1 mA	1.2 mA	10 mA
Current DAC Resolution	5-bit	5-bit	10-bit	6-bit
Waveform	Symmetric/ Asymmetric Chopped Biphasic	Biphasic	Biphasic	Symmetric Chopped Biphasic
Charge Balancing	Chopped Pulse based & Automatic Electrode Shorting	Anodic Pulse Modulation & Electrode Shorting	Pulse Insertion	Pulse Insertion
Residual potential after charge balancing	< 3 mV	< 22 mV	< 30 mV	-
Power Efficiency	50% @ 20% stimulation duty ratio	44.8% @ 20% stimulation duty ratio	-	36-51% @ 20% stimulation duty ratio
Process	0.18-µm Standard CMOS	0.18-µm Standard CMOS	0.18-µm 24V LDMOS	0.18-µm HV CMOS
Area	0.095 mm^2	0.11 mm^2	0.105 mm^2	3.36 mm^2 (include PAD)

▪ CONCLUSION

- A current-mode neural stimulator IC with novel active charge balancing technique using chopped pulse waveform and a simple charge balancer circuit is proposed and designed using 0.18-µm standard CMOS process.

▪ ACKNOWLEDGEMENTS

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▪ REFERENCE

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